9-14-04

torney's Docket No. <u>67,200-549</u>

PATENT

Group Art Unit: 1756

Examiner: Nicole M. Barreca

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re application of: Ching-Tien Ma

Serial No.: 10/038,800

Dec. 31, 2001 Filed:

For:

Method for Forming Via and Contact Holes with Deep UV Photoresist

Commissioner for Patents Alexandria, VA 22313

TRANSMITTAL OF APPEAL BRIEF (PATENT APPLICATION-37 CFR 192)

1. Transmitted herewith, in triplicate, is the APPEAL BRIEF in this application, with respect to the Notice of Appeal filed on March 12, 2004.

"The Appellant shall, within 2 months from the date of the notice of appeal under §1.191(a) or within the time NOTE: allowed for response to the action appealed from, if such time is later, file a brief in "triplicate", 37 C.F.R. 1.192(a) [emphasis added].

2.	STAT	US C)F AP	PLI	CANT

This application is on behalf of:

other than a small entity.

a small entity.

A verified statement:

is attached.

was already filed.

FEE FOR FILING APPEAL BRIEF 3.

Pursuant to 37 CFR 1.17(f), the fee for filing the Appeal Brief is:

small entity

\$165.00

other than a small entity

\$330.00

Appeal Brief fee due: \$ 330.00

Certificate of Mailing/Transmission (37 CFR 1.8(a))

I hereby certify that this correspondence is, on the date shown below, being:

Mailing

X deposited with the U.S. Postal Service with sufficient postage as Express Mail Label No. EV 305 399 530 US_ in an envelope addressed to Commissioner for Patents, Alexandria, VA 22313

(Transmittal of Appeal Brief - page 1 of 3)

NOTE:			in 37 CFR 1.192(a) are subje Notice of November 5, 1985	ct to the provision of \$\Pi\$1.136 (1060 O.G. 27).	for patent applications. 37			
The pr	roceeding	gs herein are for	a patent application and the	e provisions of 37 CFR 1.1	36 apply:			
			(complete (a) or (b), as ap	plicable)				
(a)		Applicant petitions for an extension of time under 37 CFR 1.136 (fees: 37 CFR 1.17(a)-(d) for the total number of months checked below:						
	0	Extension (months) one month two months three months four months	Fee for other than	Fee for small entity \$ 55.00 \$210.00 \$475.00 \$740.00				
				Fee	e: \$			
If an a	dditional	extension of tin	ne is required, please consi	der this a petition therefor.				
		(check	and complete the next iter	n, if applicable)				
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(b)		petit	ion is being made to provid	nsion of term is required. He for the possibility that appoin and fee for extension o	plicant has inadvertently			
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	A dun	licate copy of th	is transmittal is attached.					

EXTENSION OF TERM

4.

5.

6.

7. FEE DEFICIENCY

NOTE: If there is a fee deficiency and there is no authorization to charge an account, additional fees are necessary to cover the additional time consumed in making up the original deficiency. If the maximum six-month period has expired before the deficiency is noted and corrected, the application is held abandoned. In those instances where authorization to charge is included, processing delays are encountered in returning the papers to the PTO Finance Branch in order to apply these charges prior to action on the cases. Authorization to charge the deposit account for any fee deficiency should be checked. See the Notice of April 7, 1986, 1065 O.G. 31-33.

X If any additional extension and/or fee is required, this is a request therefor to charge Visa Credit Card No. 4756 8461 9568 0263

And/Or

X If any additional fee for claims is required, please charge Visa Credit Card No. 4756 8461 9568 0263

Signature of Attorney

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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE BEFORE THE BOARD OF PATENT APPEALS AND INTERFERENCES

Applicant: Ching-Tien Ma

Group Art Unit: 1756

Serial No.:

10/038,800

Examiner: Nicole M. Barreca

Filed:

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For:

Method for Forming Via and Contact Holes with

Deep UV Photoresist

Attorney Docket No.: 67,200-549

EXPRESS MAIL CERTIFICATE

"Express Mail" label number <u>EV 305 399 530 US</u>
Date of Deposit <u>May 12, 2004</u>

I hereby certify that this paper in triplicate and a credit card payment form in the amount of \$330.00 (required filing fee) are being deposited with the United States Postal Service "Express Mail Post Office to Addressee" service under 37 CFR §1.10 on the date indicated above and is addressed to: Mail Stop: Appeal Brief, Commissioner for Patents, P.O. Box 1450,

Alexandria, VA 22313-1450

APPEAL BRIEF

Commissioner for Patents P.O. Box 1450 Alexandria, VA 22313-1450

Sir:

Appellants appeal in the captioned application from the Examiner's final rejection dated Dec. 12, 2003, of claims 1-15 under 35 USC §103(a) over Shields '646, Suzuki '459 and Hsia '724.

It is urged that the rejection be reversed and that all the claims be allowed.

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(1) REAL PARTY IN INTEREST

The real party in interest in the present appeal is the recorded Assignee of Taiwan Semiconductor Manufacturing Company, Ltd.

(2) RELATED APPEALS AND INTERFERENCES

There are no other appeals or interferences that are known to the Appellants, the Appellants' legal representative, or the assignee.

(3) STATUS OF CLAIMS

Claims 1-15 are pending in the application.

Claims 1-15 stand rejected.

(4) STATUS OF AMENDMENTS

A Request For Reconsideration was filed on or about Feb. 17, 2004. No claim amendments were contained in the Request For Reconsideration.

An Advisory Action dated March 12, 2004 from the Examiner maintained the rejection of claims 1-15.

A Notice of Appeal was filed on or about March 12, 2004.

(5) SUMMARY OF THE INVENTION

The present invention generally relates to a method for forming via and contact holes in an insulating material layer situated on a semiconductor substrate and more particularly, relates to a method for forming via and contact holes in an insulating material layer on top of a semiconductor substrate with improved aspect ratios by using deep UV photoresist.

(Specification, page 1, lines 4-9)

In a preferred embodiment, a method for forming via openings or contact holes with improved aspect ratios by using deep UV photoresist can be carried out by the operating steps of providing a pre-processed semiconductor substrate; depositing a Sicontaining etch stop layer on top of the substrate; depositing an oxide layer on the etch stop layer; depositing a deep UV photoresist on top of the oxide layer; curing the deep UV photoresist layer with UV radiation for at least 1 min; defining openings for the via or contact; and etching the openings forming the via or contact holes.

(Specification, page 8, line 13 through page 9, line 4)

(6) ISSUES

Issue I

Is the rejection of claims 1-6 and 8-15 under 35 USC §103(a) as being unpatentable over Shields in view of Suzuki proper when such references do not teach or suggest the specifically claimed limitations in the present application?

Issue II

Is the rejection of claim 7 under 35 USC §103(a) as being unpatentable over Shields, Suzuki and Hsia proper when such references do not teach or suggest the specifically claimed limitations in the present application?

(7) GROUPING OF CLAIMS

The rejection of claims 1-6 and 8-15 are contested as a group.

The rejection of claim 7 is contested as a separate group.

The claims stand or fall together within their respective groups.

(8) ARGUMENTS

Issue I

Claims 1-6 and 8-15 are rejected under 35 USC §103(a) as being unpatentable over Shields '646 publication in view of Suzuki '459.

The rejection of claims 1-6 and 8-15 under 35 USC §103(a) based on Shields and Suzuki is improper and must be reversed.

Shields discloses a silicon oxynitride anti-reflective coating for metal patterning in which a silicon oxynitride ARC/hard mask is formed on a metal layer and patterned, avoiding a separate hard mask. In the Shields' process, a thin silicon oxide layer is formed on top of the silicon oxynitride layer in order to improve resistance to footing. As stated at page 3, left column, lines 6-8:

"Silicon oxide layer 36 can be formed at a thickness of about 20 angstrom to about 300 angstrom without significantly increase the height of the stack".

The Appellants respectfully submit that Shields teaches a completely different process of forming metal lines when compared to the present invention process of forming a deep via with large aspect ratio in a silicon oxide layer. For instance, at page 14 of the specification, lines 15+:

"As shown in Figure 3, the depth of the via openings 40, shown as " L_2 " is measured to be 639 nm, which represents a 40% improvement over that obtained by the conventional method shown in Figure 2".

The thickness of the silicon oxide layer, into which the deep via opening is formed, is therefore at least 6400 angstrom, when compared to the silicon oxide layer of Shields at 20-300 angstroms. Shields therefore does not teach the present invention process of forming a deep via with high aspect ratios. As a matter of fact, Shields not only does not teach a method for forming a deep via, or for that matter, a method for forming a via at all, it is simply impossible to form any via in the Shields' structure. While the Examiner contended at page 3 of the 12/12/2003 Office Action that Shields provides a "stack" that has a total height of about 13,000 angstroms, the height is mainly made up of a photoresist layer (900 angstrom), a barrier metal layer (750 angstrom) and a metal layer (8,000 angstrom), it is simply

impossible to form an electrically conductive via in these layers.

A via can only be formed in a dielectric or insulating material layer such as that of silicon oxide, normally known as inter-metal dielectric layer. The silicon oxide layer taught by Shields has a thickness of about 20 - 300 angstrom such that it is simply out of the question that a via can be formed in such an oxide layer. The Applicants further submit that while Suzuki teaches curing a photoresist with UV radiation, Suzuki does not lend any additional weight in a §103 rejection of claims 1-6 and 8-15 since the basic deep via forming process is not taught by either Shields or Suzuki, either singularly or in combination thereof.

The rejection of claims 1-6 and 8-15 under 35 USC §103(a) based on Shields and Suzuki is improper and must be reversed.

Issue II

Claim 7 is rejected under 35 USC §103(a) as being unpatentable over Shields, Suzuki and further in view of Hsia '724. It is contended that Hsia teaches that in a conventional metallization process, it is known that a chemical compound film will be formed on the metal layer during the etching process as a result of a reaction between the hydrocarbon polymers of the

photoresist and the chlorine or fluorine molecules contained in the reactive ion etching chemicals.

The rejection of claim 7 under 35 USC §103(a) based on Shields, Suzuki and Hsia is improper and must be reversed.

Claim 7 depends on independent claim 1, which the Appellants have clearly shown is not taught by the two primary references of Shields and Suzuki. The Appellants further submit that the additional reference of Hsia does not lend any additional weight in a §103 rejection, since Hsia does not teach the forming of a via at all.

The rejection of claim 7 under 35 USC §103(a) based on Shields, Suzuki and Hsia is improper and must be reversed.

CLOSING

In summary, the Appellants have shown that their claimed invention is fully supported by a body of evidence of non-obviousness. It is therefore respectfully submitted that such evidence of non-obviousness overcomes any showing of obviousness presented by the Examiner. The Appellants therefore submit that

the final rejection of their claims 1-15 is improper under 35 USC \$103(a).

The reversal of the final rejection is respectfully solicited from the Board.

Respectfully submitted,

Randy W. Tung

Registration No. 31,311

CLAIM APPENDIX

1. (original) A method for forming via or contact holes with improved aspect ratios by using deep UV photoresist comprising the steps of:

providing a pre-processed semiconductor substrate;

depositing a Si-containing etch stop layer on top of said substrate;

depositing an oxide layer on said etch stop layer;

depositing a deep UV photoresist on top of said oxide layer;

curing said deep UV photoresist with UV radiation for at least

1 minute;

defining openings for said via or contact; and etching said openings forming said via or contact holes.

2. (original) A method for forming via or contact holes with improved aspect ratios by using deep UV photoresist according to claim 1 further comprising the step of etching said openings to form via or contact holes having an aspect ratio of at least 8.

- 3. (original) A method for forming via or contact holes with improved aspect ratios by using deep UV photoresist according to claim 1 further comprising the step of depositing said Sicontaining etch stop layer with a material selected from the group consisting of Si_3N_4 , SiON and SiC.
- 4. (original) A method for forming via or contact holes with improved aspect ratios by using deep UV photoresist according to claim 1, wherein said oxide layer deposited is an inter-level-dielectric (ILD) layer.
- 5. (original) A method for forming via or contact holes with improved aspect ratios by using deep UV photoresist according to claim 1 further comprising the step of curing said deep UV photoresist with UV radiation for a time period between about 1 minute and about 10 minutes.
- 6. (original) A method for forming via or contact holes with improved aspect ratios by using deep UV photoresist according to claim 1 further comprising the step of curing said deep UV photoresist with UV radiation for a time period between about 1 minute and about 10 minutes at a temperature of at least 100°C.

- 7. (original) A method for forming via or contact holes with improved aspect ratios by using deep UV photoresist according to claim 1 further comprising the step of reducing fluorocarbon polymer formation from said deep UV photoresist by curing with UV radiation.
- 8. (original) A method for forming via or contact holes with improved aspect ratios by using deep UV photoresist according to claim 1 further comprising the step of removing said Si-containing etch-stop layer.
- 9. (previously presented) A method for forming a large aspect ratio hole in an insulating material layer on a semi-conducting substrate comprising the steps of:

providing a pre-processed semi-conducting substrate having an etch-stop layer deposited on top;

depositing an insulating material layer on said etch-stop layer;

forming a deep UV photoresist layer on top of said insulating material layer;

irradiating said deep UV photoresist layer with UV radiation for at least 1 minute;

defining an opening for a hole;

etching said hole having an aspect ratio of larger than 8 in said insulating material layer by using said deep UV photoresist layer; and

removing said etch-stop layer in said etched hole.

- 10. (original) A method for forming a large aspect ratio hole in an insulating material layer on a semi-conducting substrate according to claim 9 further comprising the step of forming the hole with an aspect ratio between about 8 and about 20.
- 11. (original) A method for forming a large aspect ratio hole in an insulating material layer on a semi-conducting substrate according to claim 9 further comprising the step of depositing said insulating material layer with an inter-level-dielectric (ILD) material.
- 12. (previously presented) A method for forming a large aspect ratio hole in an insulating material layer on a semi-conducting substrate according to claim 9 further comprising the step of depositing said insulating material layer in silicon oxide.

- 13. (original) A method for forming a large aspect ratio hole in an insulating material layer on a semi-conducting substrate according to claim 9 further comprising the step of depositing said etch-stop layer by a material selected from the group consisting of Si_3N_4 , SiON and SiC.
- 14. (original) A method for forming a large aspect ratio hole in an insulating material layer on a semi-conducting substrate according to claim 9 further comprising the step of irradiating said deep UV photoresist layer with UV radiation for a time period between about 1 minute and about 10 minutes.
- 15. (original) A method for forming a large aspect ratio hole in an insulating material layer on a semi-conducting substrate according to claim 9 further comprising the step of etching said hole for forming a via or a contact.